## REMARKS

The Applicants respectfully request reconsideration of this Application. The Applicants originally submitted Claims 1-15 in the Application. The Applicants have previously amended Claims 1-8 and 10-14 and have canceled Claims 4, 9, 14 and 15. The Applicants have presently amended Claims 1 and 10. No claims have been added. Accordingly, Claims 1-3, 5-8 and 10-13 are currently pending in the Application.

### I. Rejection of Claims 1-3, 5-8 and 10-13 under 35 U.S.C. §112

The Examiner has rejected Claims 1-3, 5-8 and 10-13 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Specifically, the Examiner believes that the language in independent Claims 1 and 10 reciting an "electrically isolated conductive trace" and an "electrically isolated conductive tester runner", respectively, are incompatible with further limitations in these claims. Although the Applicants do not necessarily agree with the Examiner, Claims 1 and 10 have been amended to more clearly recite the structure of the claimed invention. Accordingly, the Applicants respectfully request the Examiner withdraw the §112, second paragraph, rejection with respect to the pending claims.

### II. Rejection of Claims 1, 2, 5-8 and 10-12 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 5-8 and 10-12 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,201,308 to Ikegami. The teachings and deficiencies of Ikegami have been discussed in the prior Amendments and will not be repeated here.

In contrast to independent Claim 1, Ikegami does not disclose a conductive trace formed at an outer region of a substrate coupled to two of a plurality of bond pads, where the trace and the bond pads are electrically isolated from interconnects used for interconnecting integrated circuit devices to form an integrated circuit. Rather, the traces disclosed in Ikegami are electrically interconnected with components and interconnections used to form an integrated circuit, and thus, are not electrically isolated therefrom. (Col. 3, lines 62-67 and Col. 4, lines 1-29). Thus, the traces in Ikegami are not for testing the strength of the traces, while remaining electrically isolated from the interconnections of integrated circuit components, as recited by Claim 1. As a result, Ikegami does not anticipate Claim 1. Since independent Claim 10, as amended, recites elements analogous to those of Claim 1, Ikegami also does not anticipate Claim 10.

In conclusion, Ikegami does not teach the inventions recited in independent Claims 1 and 10 and, as such, is not an anticipating reference for these claims. In addition, dependent Claims 2, 5-8 and 11-12 depend from Claims 1 and 10, respectively. Thus, Ikegami is also not an anticipating reference for these dependent claims. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to the pending claims.

## III. Rejection of Claims 3 and 13 under 35 U.S.C. §103

The Examiner has rejected dependent Claims 3 and 13 under 35 U.S.C. §103(a) as being unpatentable over Ikegami, as applied above, in view of U.S. Patent No. 5,811,874 to Lee. The Applicants respectfully assert that the claimed invention is nonobvious in view of the combination of the foregoing references, and that the combination does not established a *prima facie* case of obviousness of dependent Claims 3 and 13.

As discussed above, Ikegami does not teach an integrated circuit having a substrate with an electrically isolated trace that is electrically isolated from interconnections and components forming the integrated circuit, as recited in independent Claims 1 and 10. In addition, Ikegami does not suggest the use of such an electrically isolated trace, since the conductive traces disclosed in Ikegami are not used for testing the integrity of internal circuitry, but rather are electrically interconnected to form the integrated circuit. In addition, Lee merely provides for chamferred regions along conductive traces to reduce the shear stress of the traces, and the Examiner has relied upon this teaching for only so much. Lee does not teach or suggest the use of those conductive traces as electrically isolated test traces, but rather as part of the overall semiconductor chip device described therein. Therefore, since the combined teachings of Ikegami and Lee fail to teach or suggest all the inventions of independent Claims 1 and 10, the combination does not establish a *prima facie* case of obviousness of dependent Claims 3 and 13, which include the elements of independent Claims 1 and 10, respectively. Accordingly, a *prima facie* case of obvious of Claims 3 and 13 has not been established, and the Applicants respectfully request the Examiner withdraw the §103 rejection of dependent Claims 3 and 13.

## IV. Conclusion

The Applicants respectfully request that the rejections be withdrawn and solicit a Notice of Allowance for Claims 1-3, 5-8 and 10-13. The Applicants further attach hereto a marked-up

version of the amendments made to the claims. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Respectfully submitted,

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**APPLICATION NO. 09/604,519**

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

(1) Claim 1 has been amended as follows:

1. (Three times amended) An integrated circuit comprising:

a substrate having interconnects for interconnecting integrated circuit devices;

a plurality of bond pads formed above the substrate; and

a first [electrically isolated] conductive trace formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads, the first conductive trace and at least two bond pads electrically isolated from the interconnects.

(2) Claim 10 has been amended as follows:

10. (Three times amended) An integrated circuit comprising:

a substrate having interconnects for interconnecting integrated circuit devices;

a plurality of bond pads; and

[an electrically isolated] a conductive tester runner formed on the substrate and around the plurality of bond pads[, the isolated conductive tester runner] and electrically coupled to at least two of the plurality of bond pads, the conductive tester runner and at least two bond pads electrically isolated from the interconnects.